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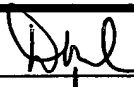
U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	A. Raghunathan, S. Dey and N. K. Jha, <i>Glitch Analysis And Reduction In Register-Transfer-Level Power Optimization</i> , IEEE Proc. of Design Automation Conference (DAC96), pp. 331-336 (1996).
	A. Chandrakasan, M. Potkonjak, J. Rabaey and R. Brodersen, <i>Hyper-LP: A System for Power Minimization using Architectural Transformations</i> , IEEE Proc. of Int'l Conf. on Computer-Aided Design (IC-CAD92), pp. 300-303 (1992).
	G. Lakshminarayana, A. Raghunathan, K. S. Khouri and N. K. Jha, <i>Common Case Computation: A High-Level Power-Optimizing Technique</i> , IEEE Proc. of Design Automation Conference (DAC99), pp. 1-6 (June 1999).
	S. Kumar, J. Aylor, B. Johnson and W. Wuif, <i>Object-Oriented Techniques in Hardware Design</i> , IEEE Computer, Vol. 27, pp. 64-70 (June 1994).
	F. Mallet, F. Hoed, and J.F. Duboc, <i>Hardware Architecture Modeling Using an Object-Oriented Method</i> , Proceedings of the 24th EUROMICRO Conference, pp. 147-153 (August 1998).

EXAMINER: DWIN CRAIG

DATE CONSIDERED: 10-24-03

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